**Interfacing Synchronous and Asynchronous Domains for Open Core Protocol**

**Abstract**

Intellectual property (IP) blocks are connected in a system on chip using a bus or network-on-chip (NoC). IP reuse is facilitated by the modularity that results when using  
common interfaces between the IP cores and the bus or NoC. This paper investigates and implements several versions of one of the common interfaces, the open core protocol (OCP). The  
paper addresses two new aspects of interface design. First, an approach is developed to partition the common protocol portion of the interface from the interface back-end which is specific to  
the particular IP. This is achieved with a component we call a domain interface at this boundary. Second, the domain interface is enhanced to synchronize between IP blocks and busses that  
use different clock frequencies or asynchronous (unclocked) logic. As a result IP operating at unrelated frequency and fully asynchronous (unclocked) blocks can more easily be integrated into a system. Results are reported for power, performance and area for these clocked and asynchronous implementations.

**Tools:**

* Modelsim 6.4b
* Xilinx ISE 10.1

**Languages:**

* VHDL/Verilog HDL